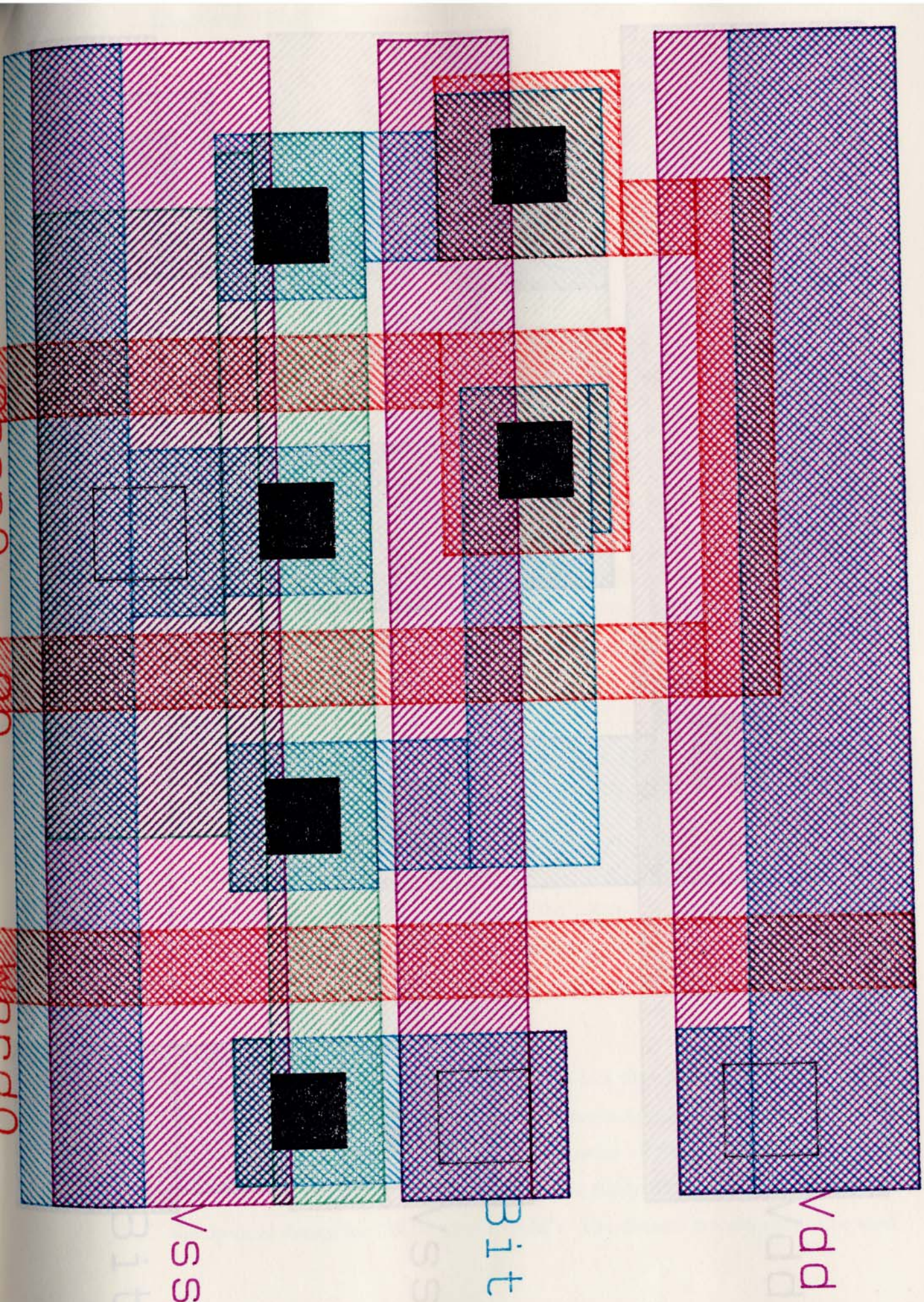

Figure 4–4: Three Transistor Dynamic RAM Layout (a).

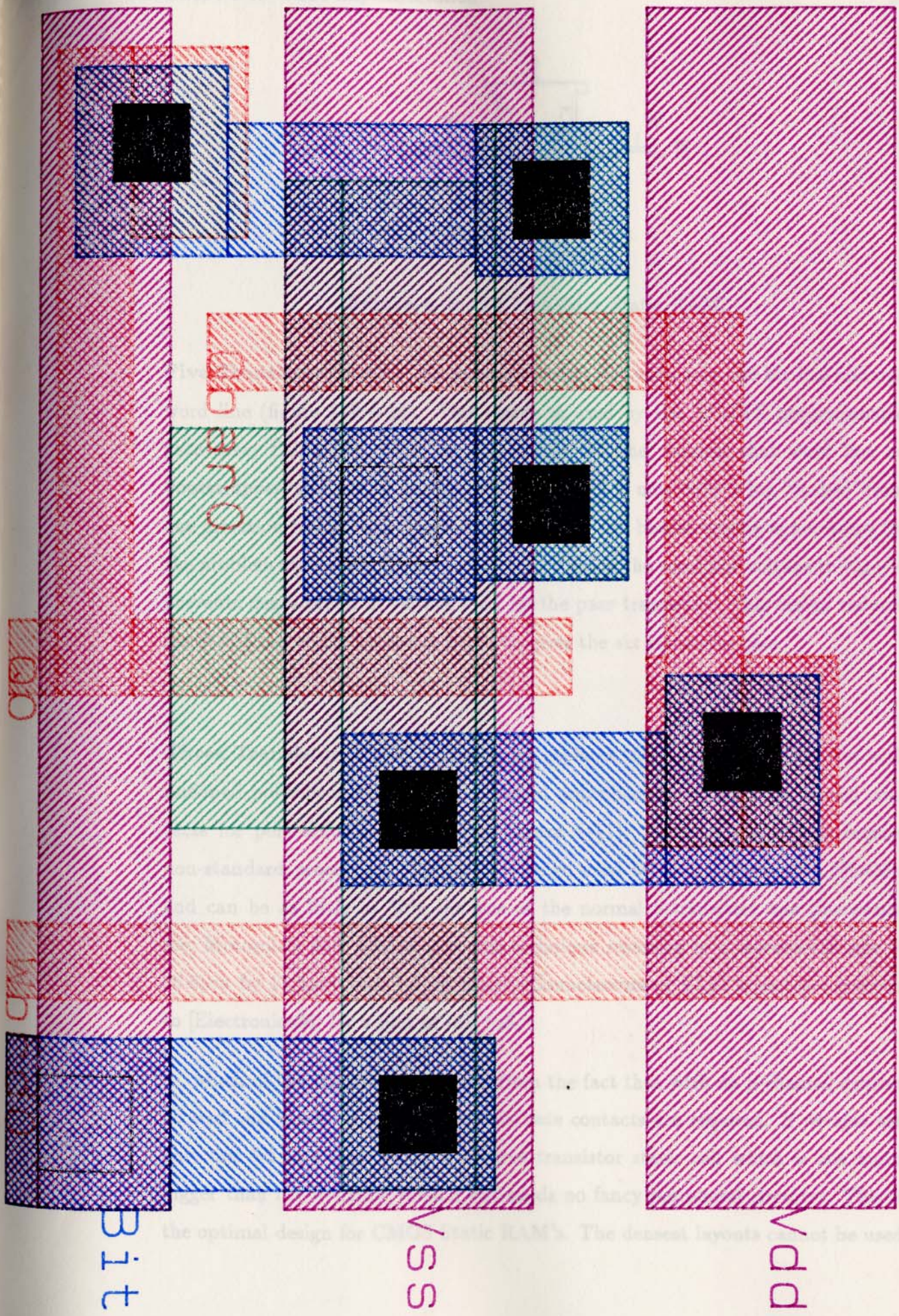

Figure 4–5: Three Transistor Dynamic RAM Layout (b).

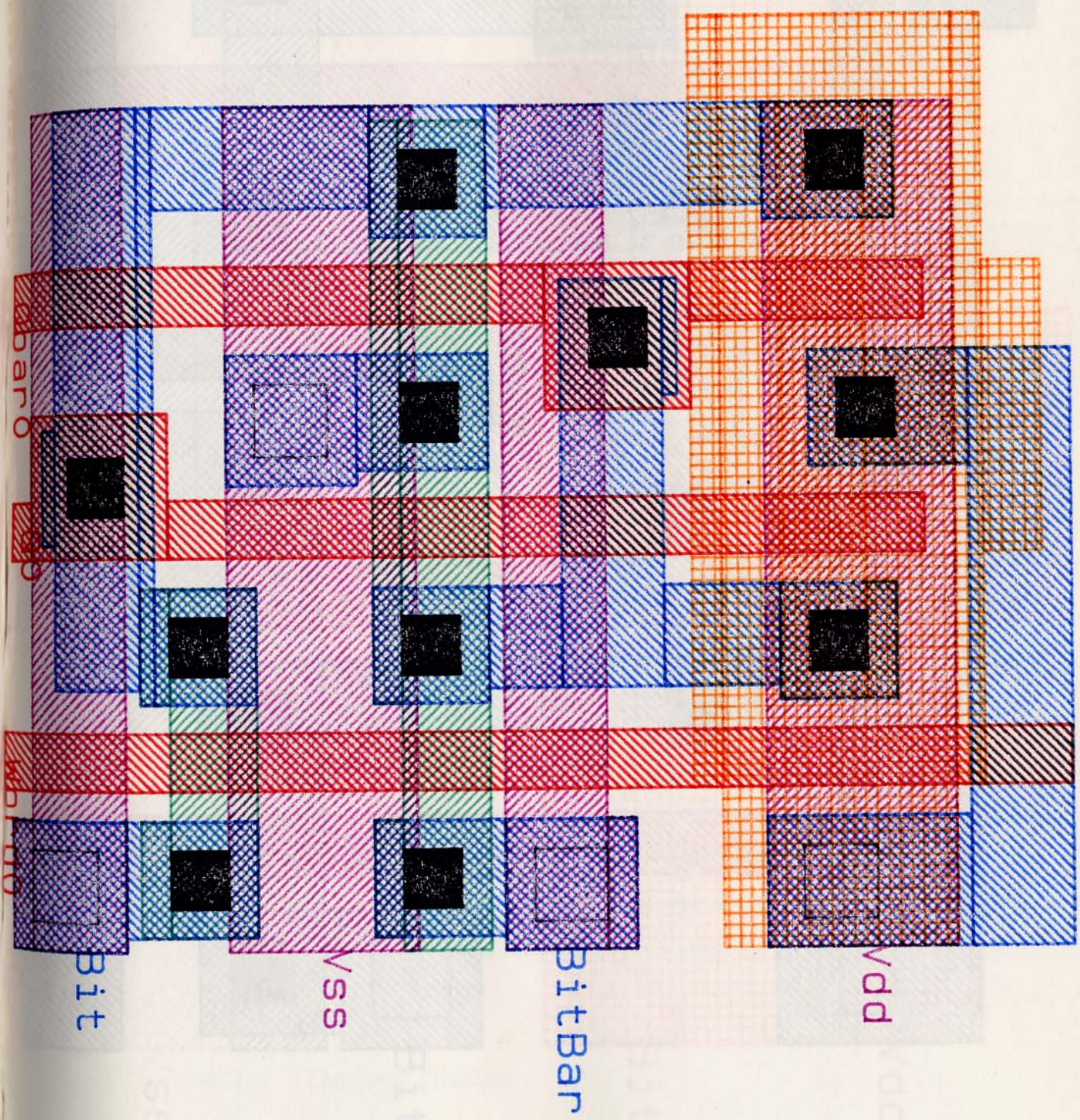

Figure 4–7: Six Transistor Static RAM Layout (a).

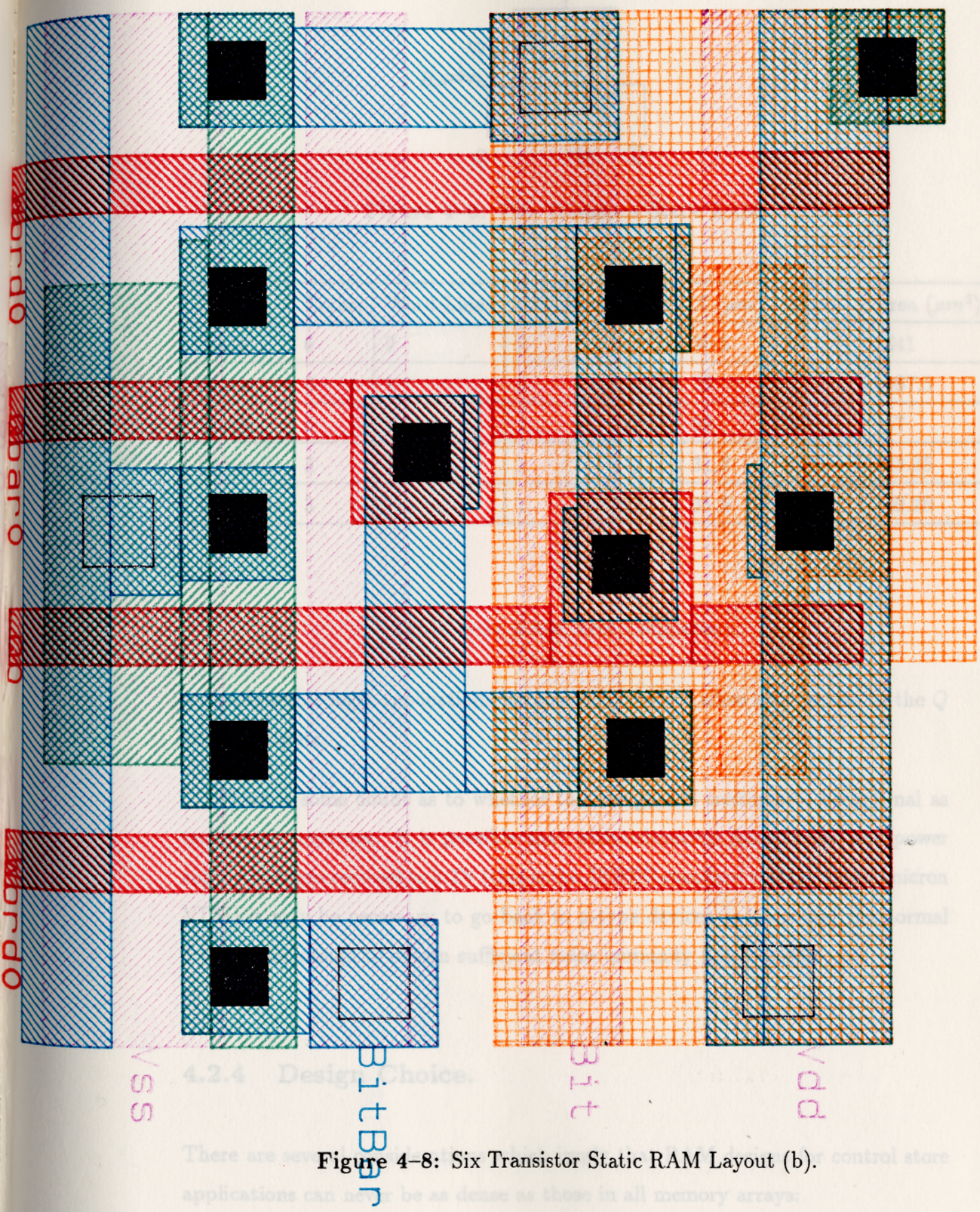

Figure 4–8: Six Transistor Static RAM Layout (b).

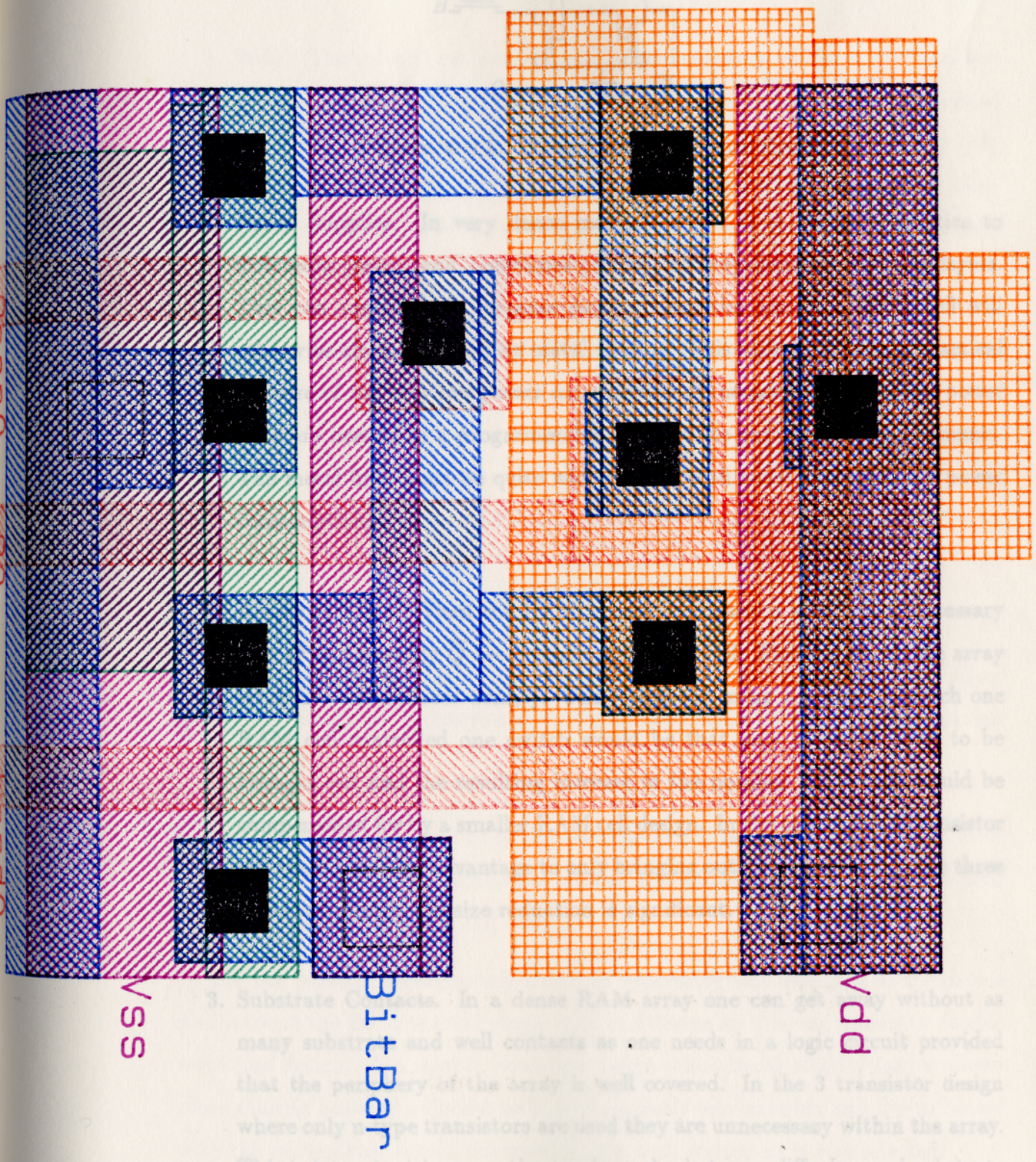

Figure 4–10: Five Transistor Static RAM Layout.

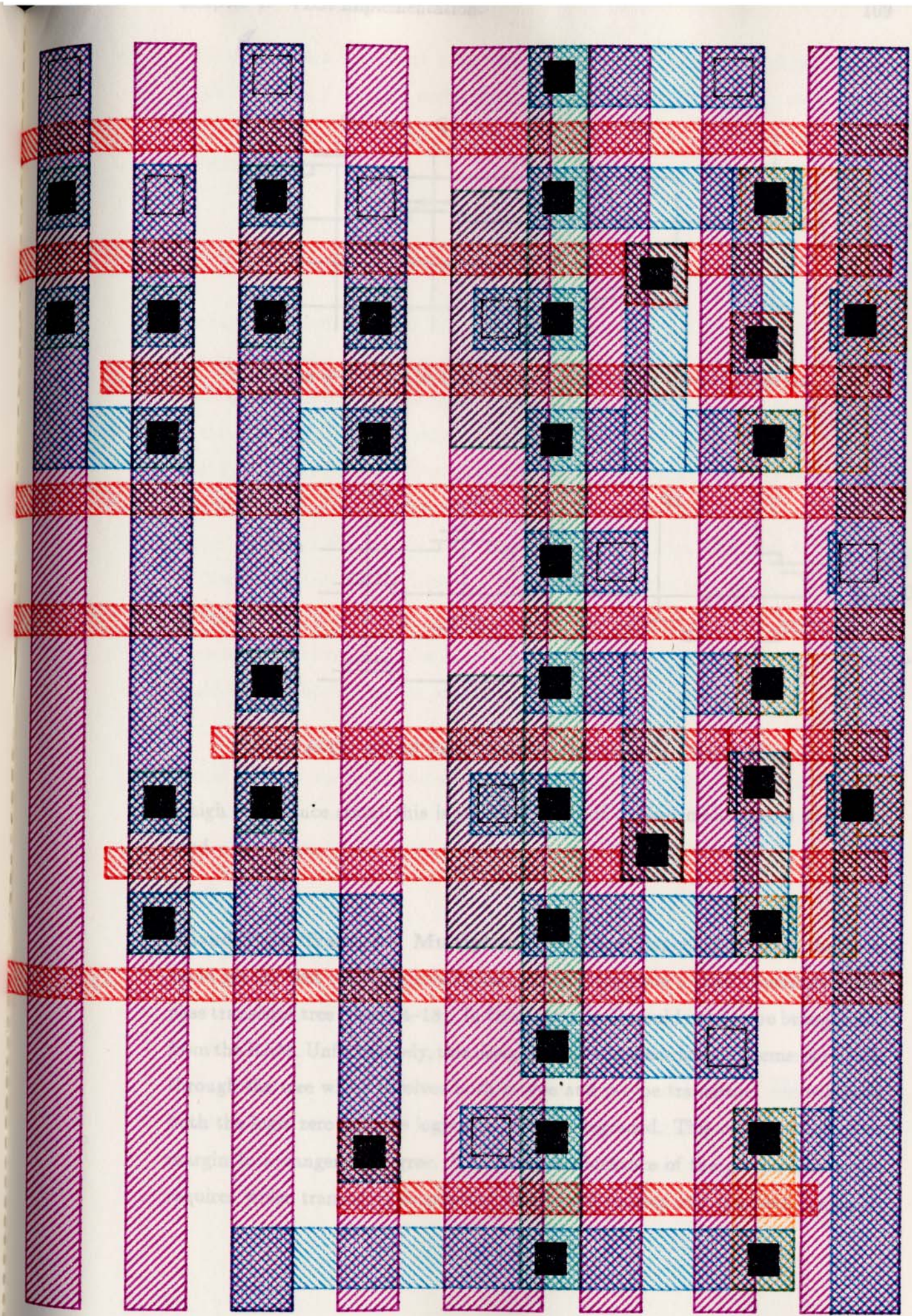

Figure 4–16: Pass Transistor Multiplexor Layout.

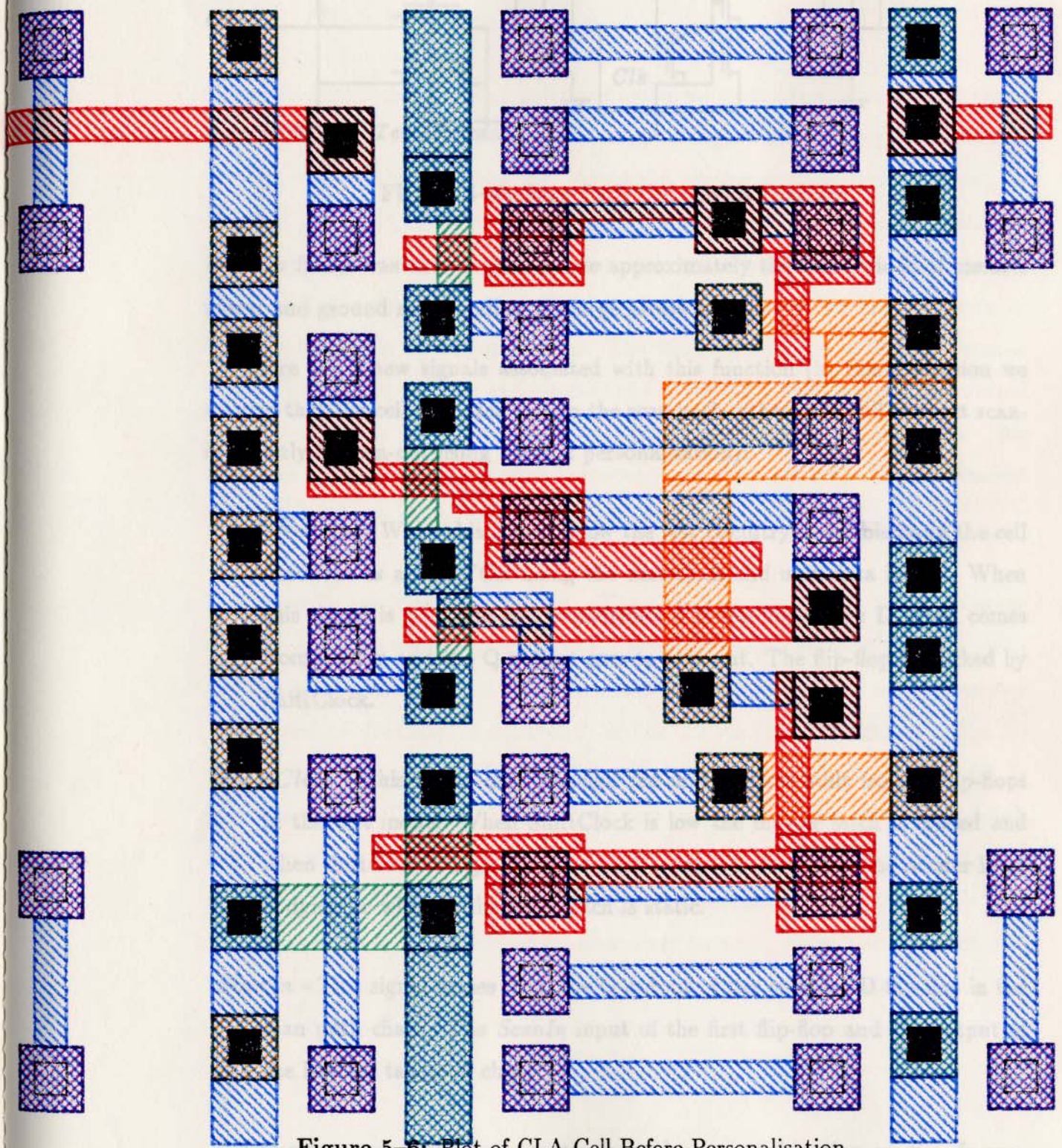

Figure 5–6: Plot of CLA Cell Before Personalisation.

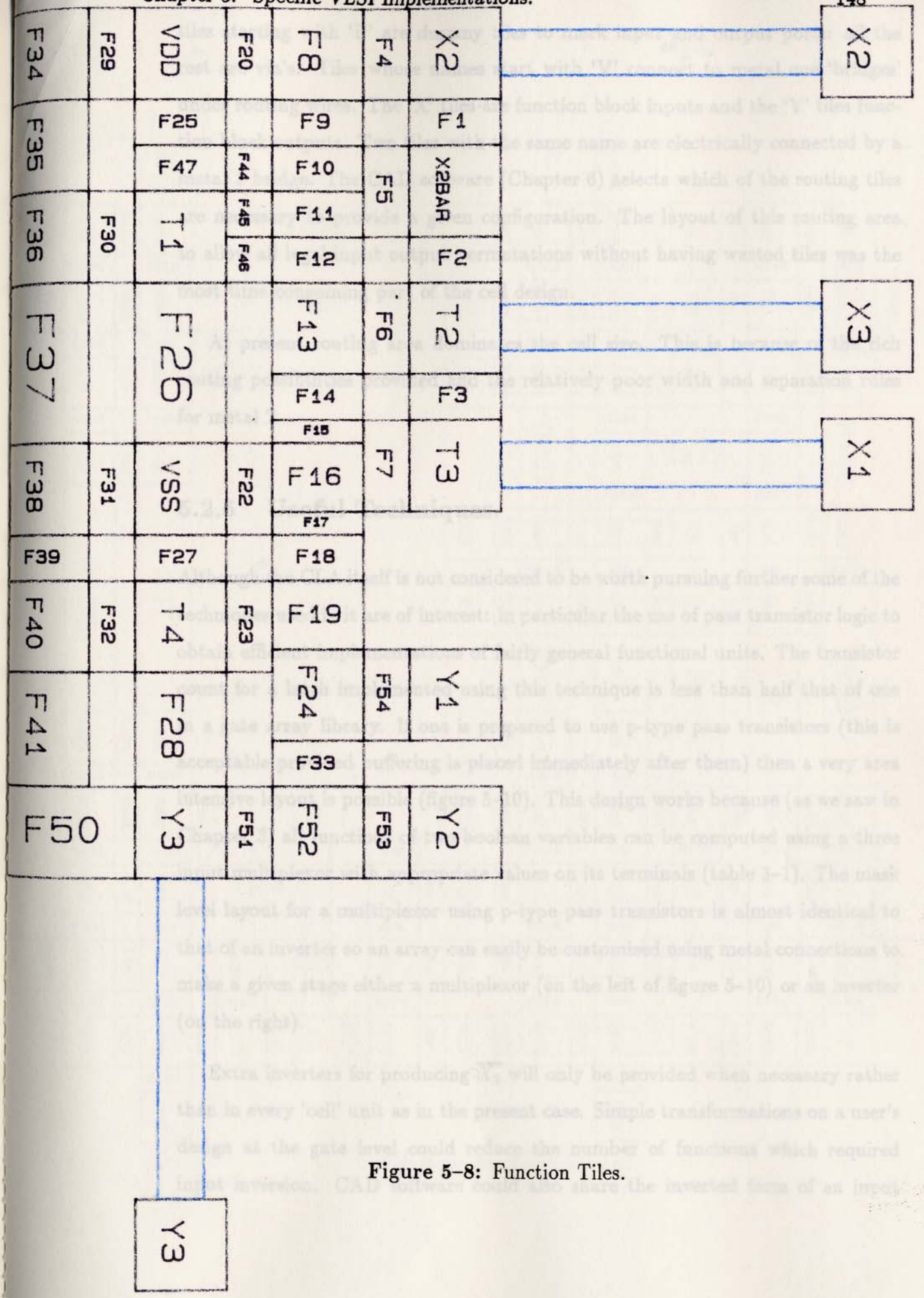

Figure 5–8: Function Tiles.

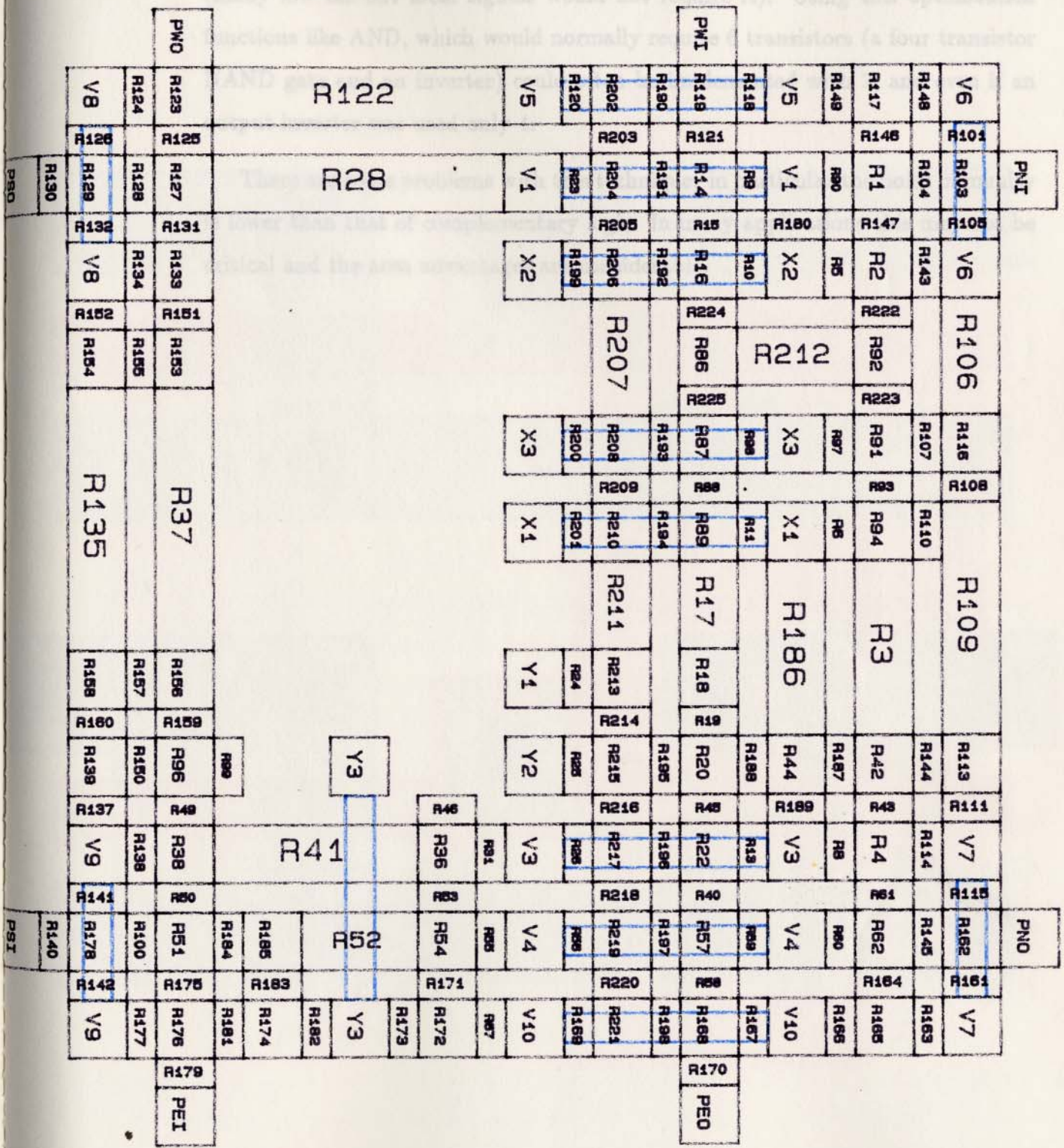

Figure 5–9: Routing Tiles.

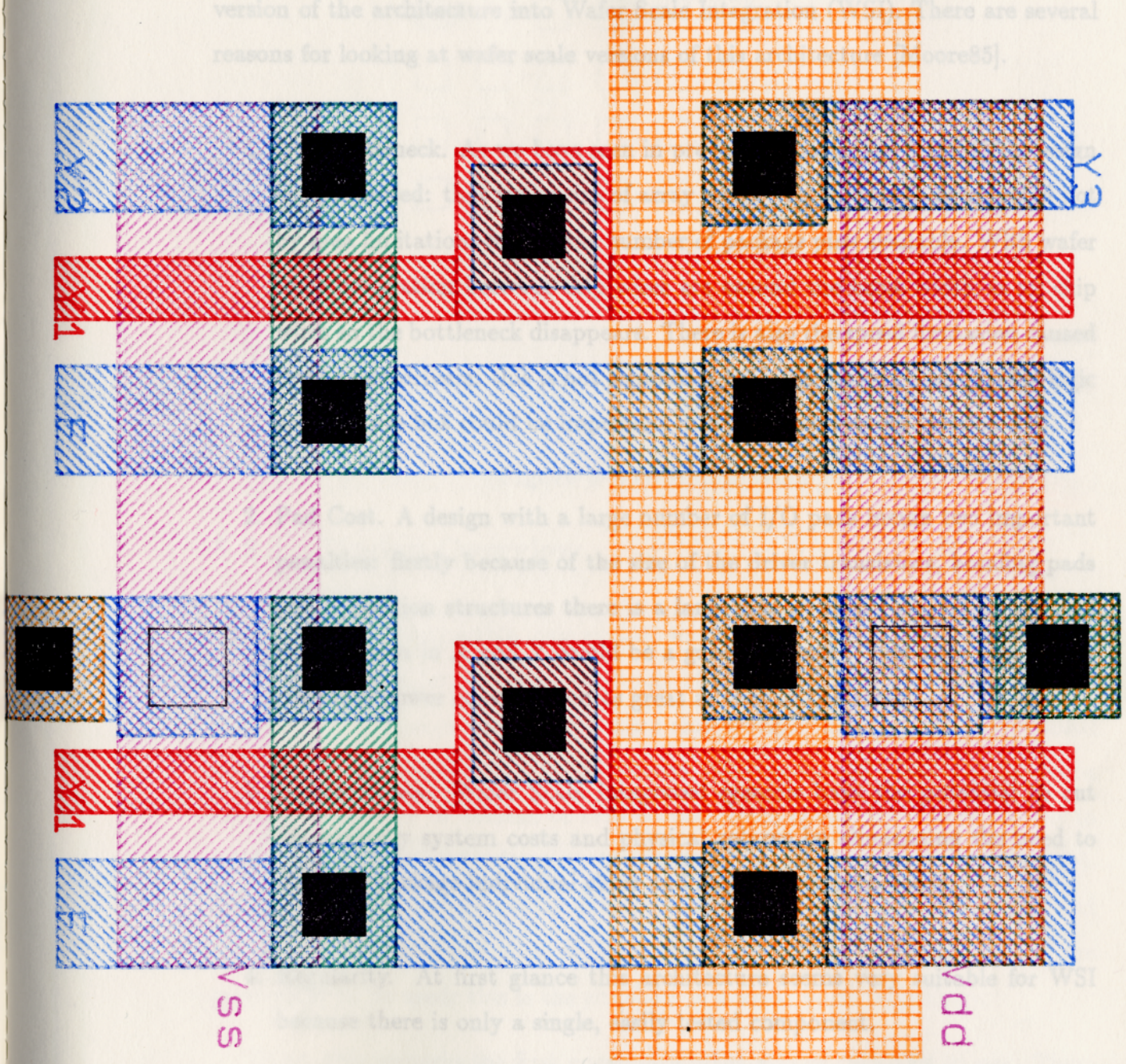

Figure 5–10: Function Block Stage Layout.