

Figure 4-4: Three Transistor Dynamic RAM Layout (a).

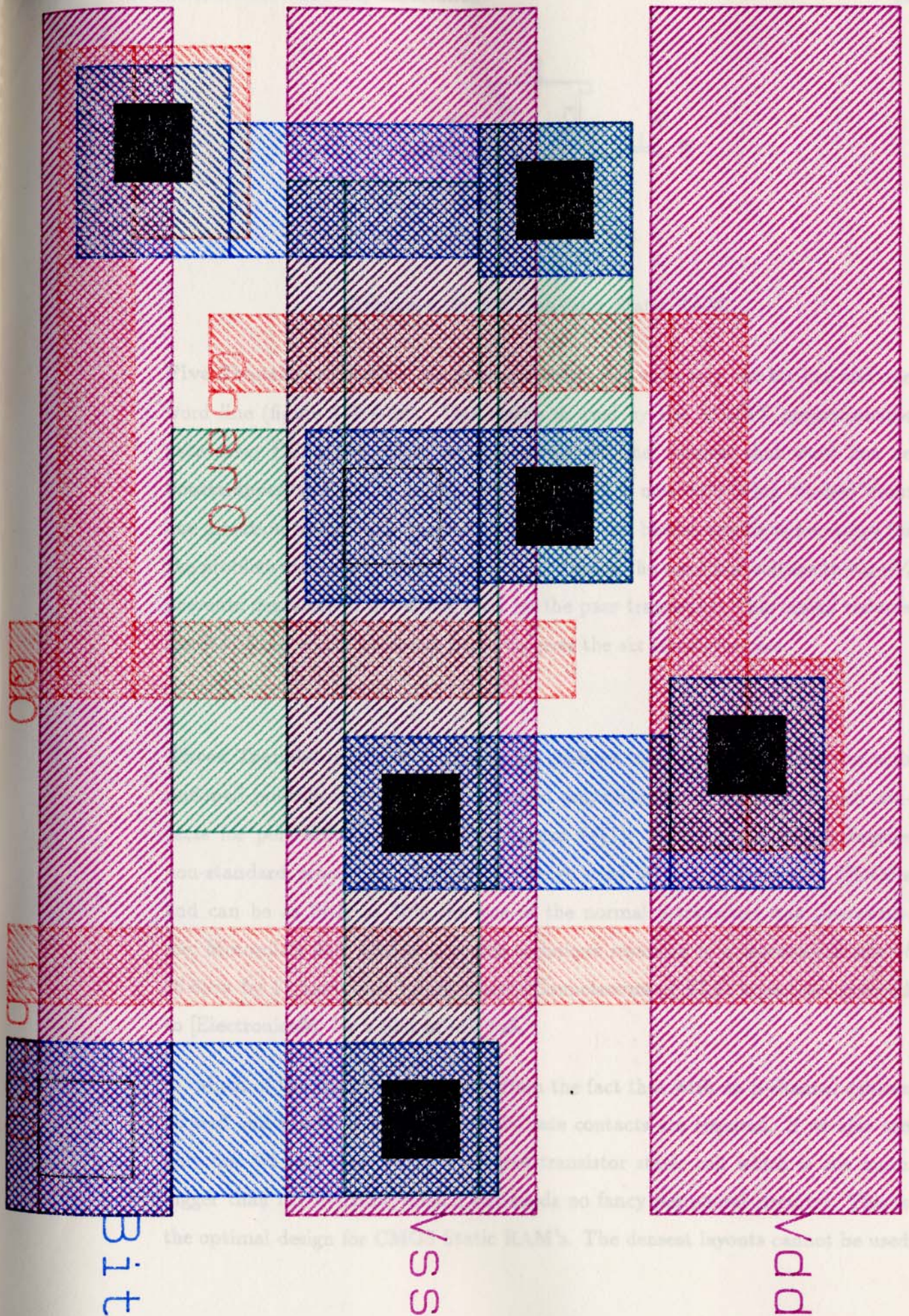


Figure 4-5: Three Transistor Dynamic RAM Layout (b).

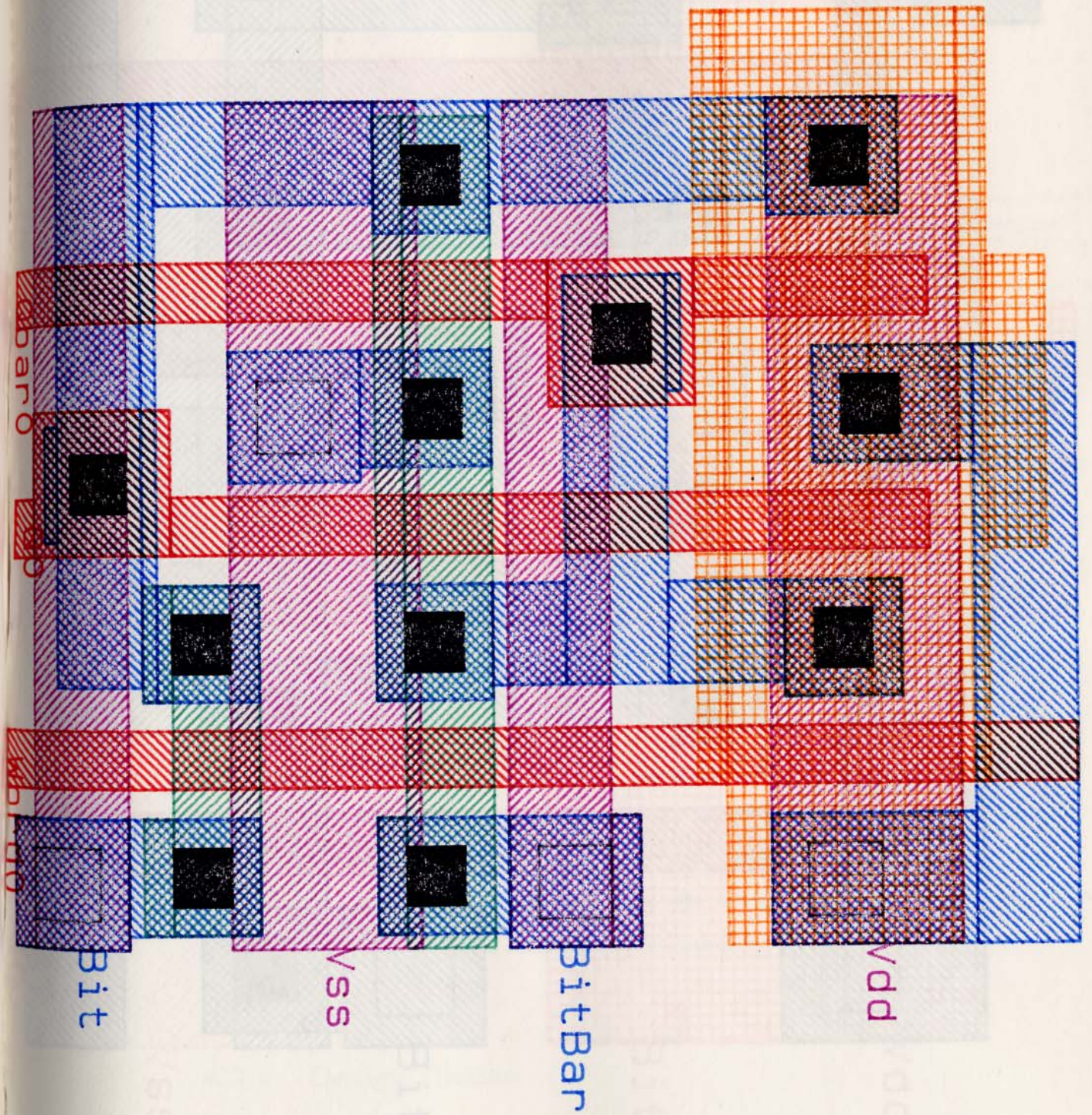


Figure 4-7: Six Transistor Static RAM Layout (a).

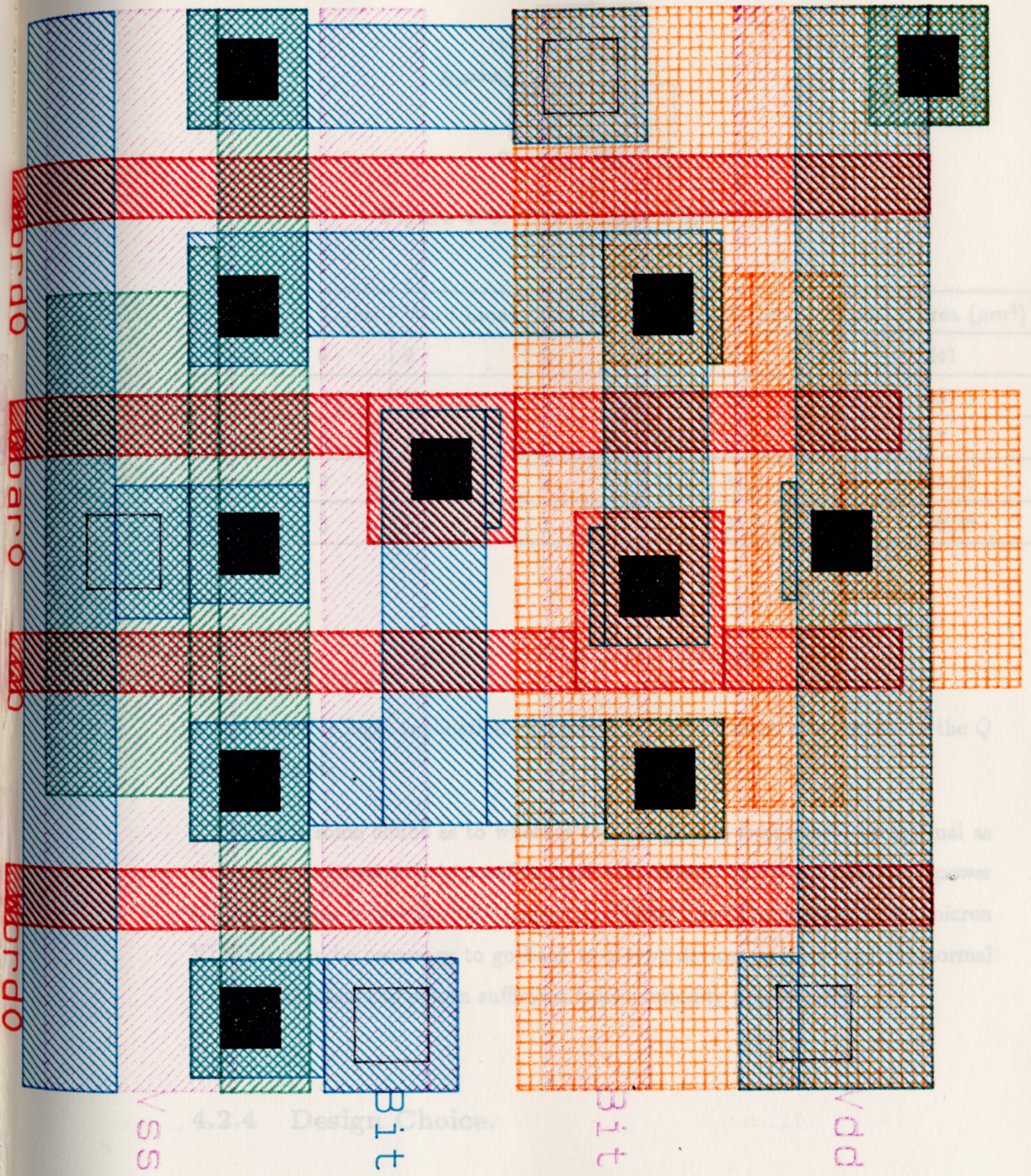


Figure 4-8: Six Transistor Static RAM Layout (b).

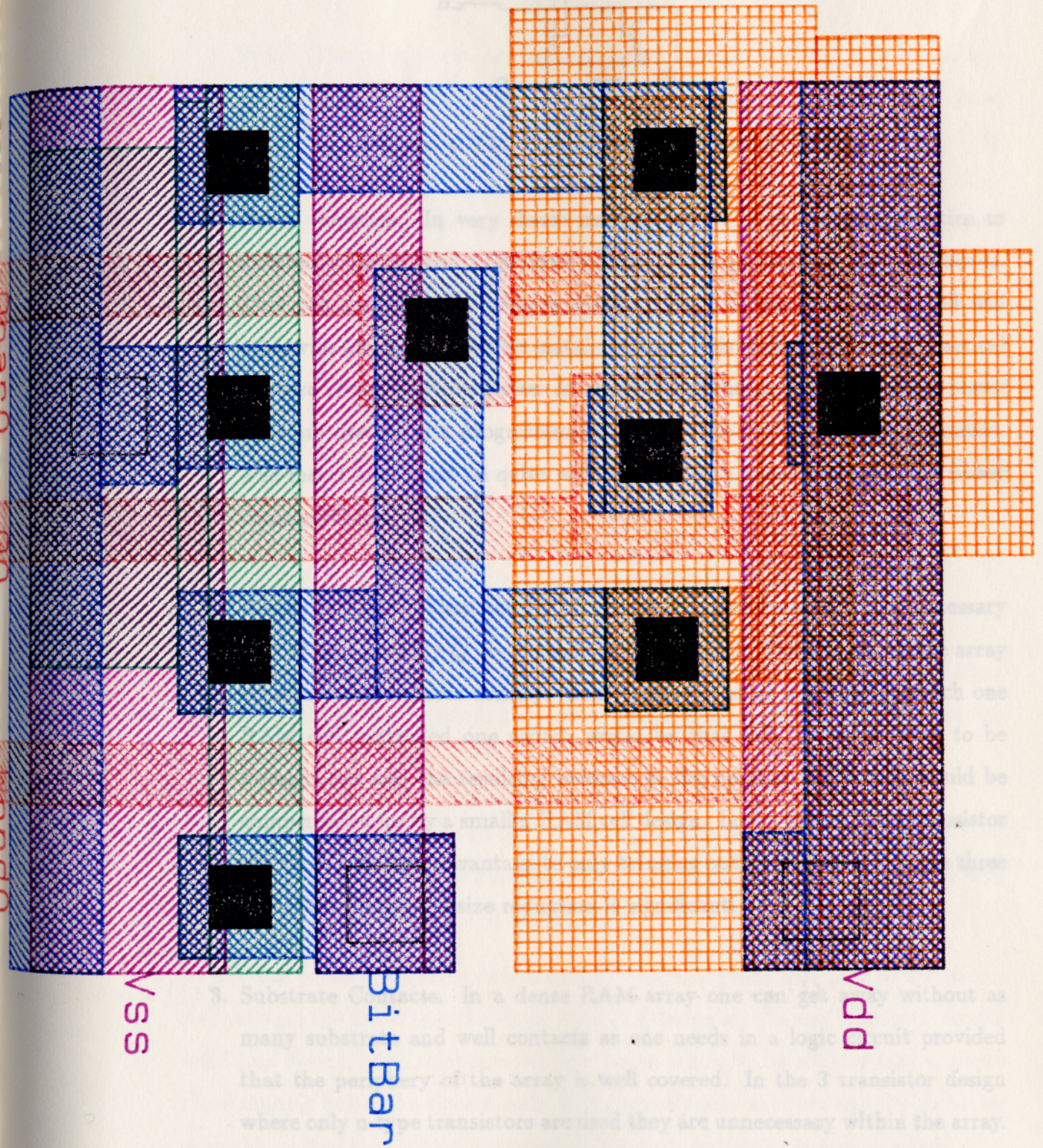


Figure 4-10: Five Transistor Static RAM Layout.

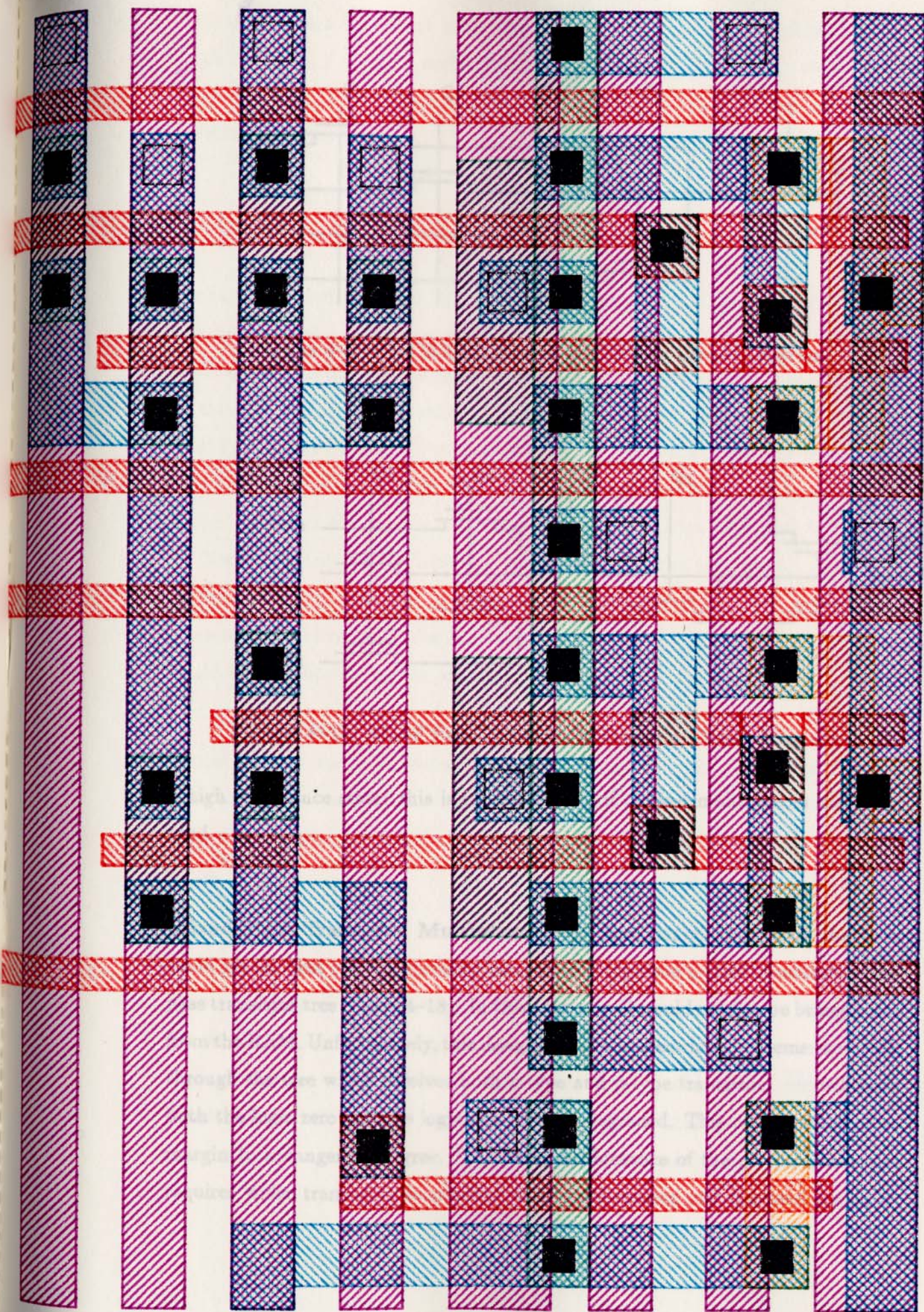


Figure 4-16: Pass Transistor Multiplexor Layout.

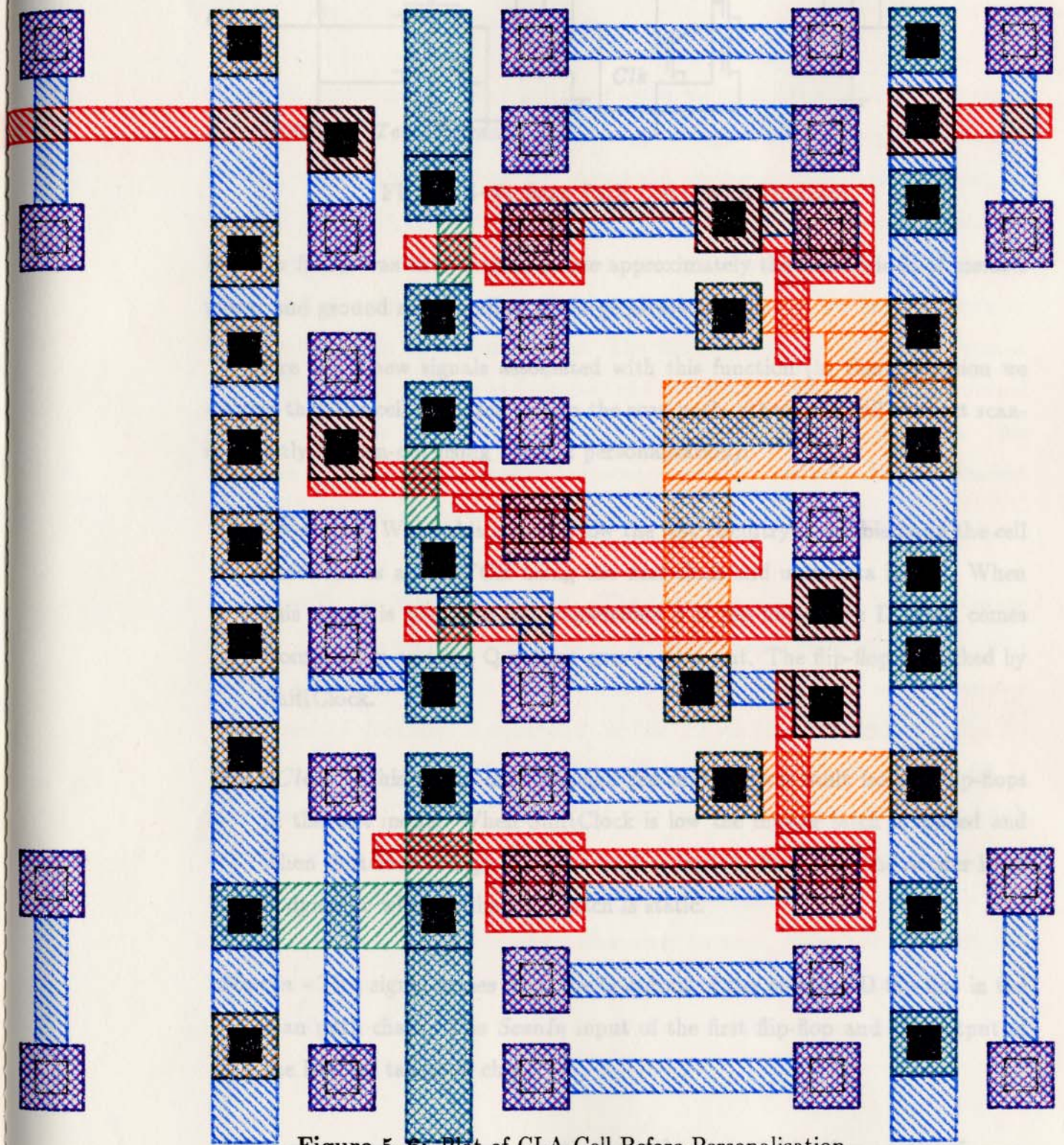


Figure 5-6: Plot of CLA Cell Before Personalisation.

considerably complicate the electrical design of the cell and must be slow to avoid

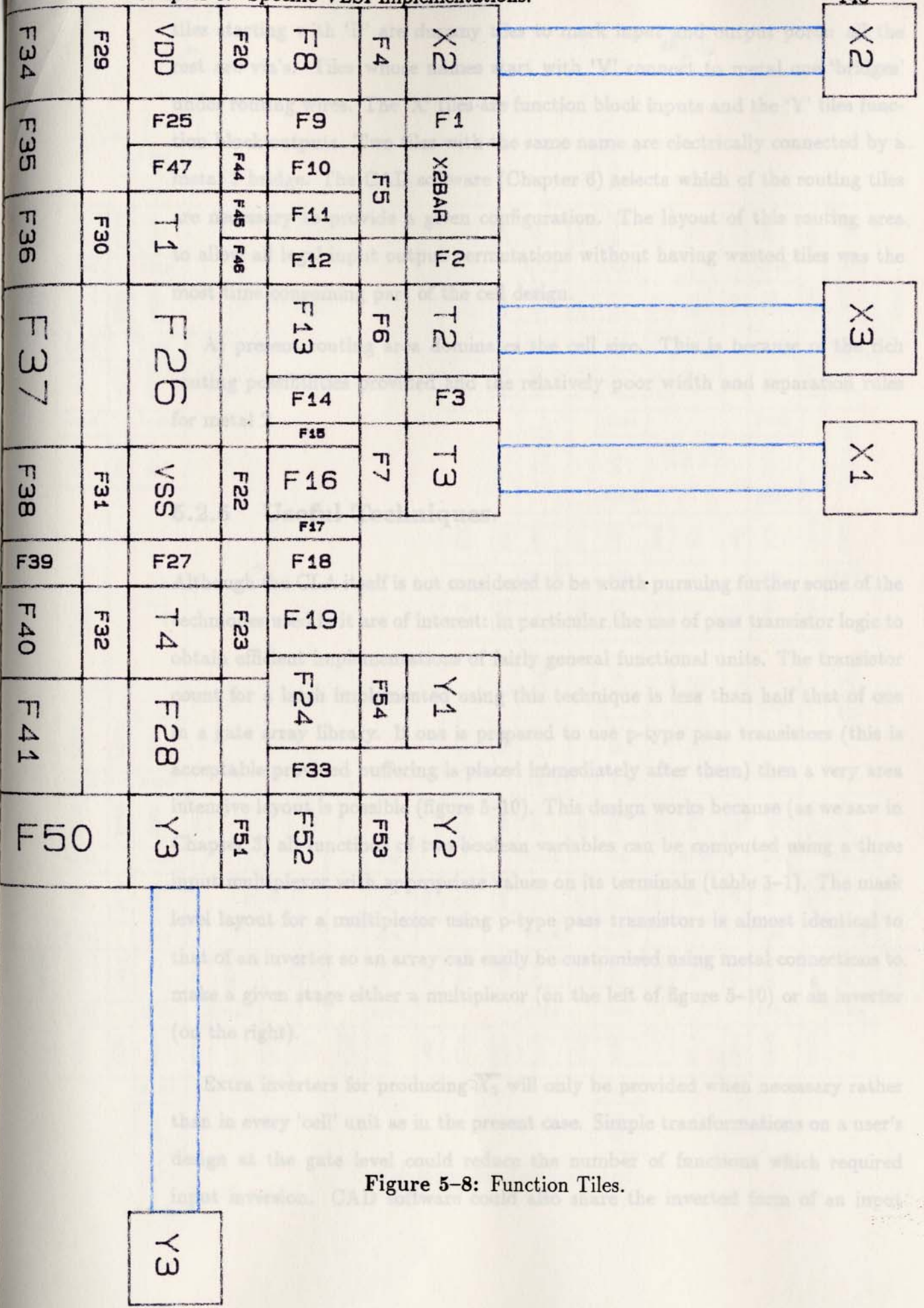


Figure 5-8: Function Tiles.



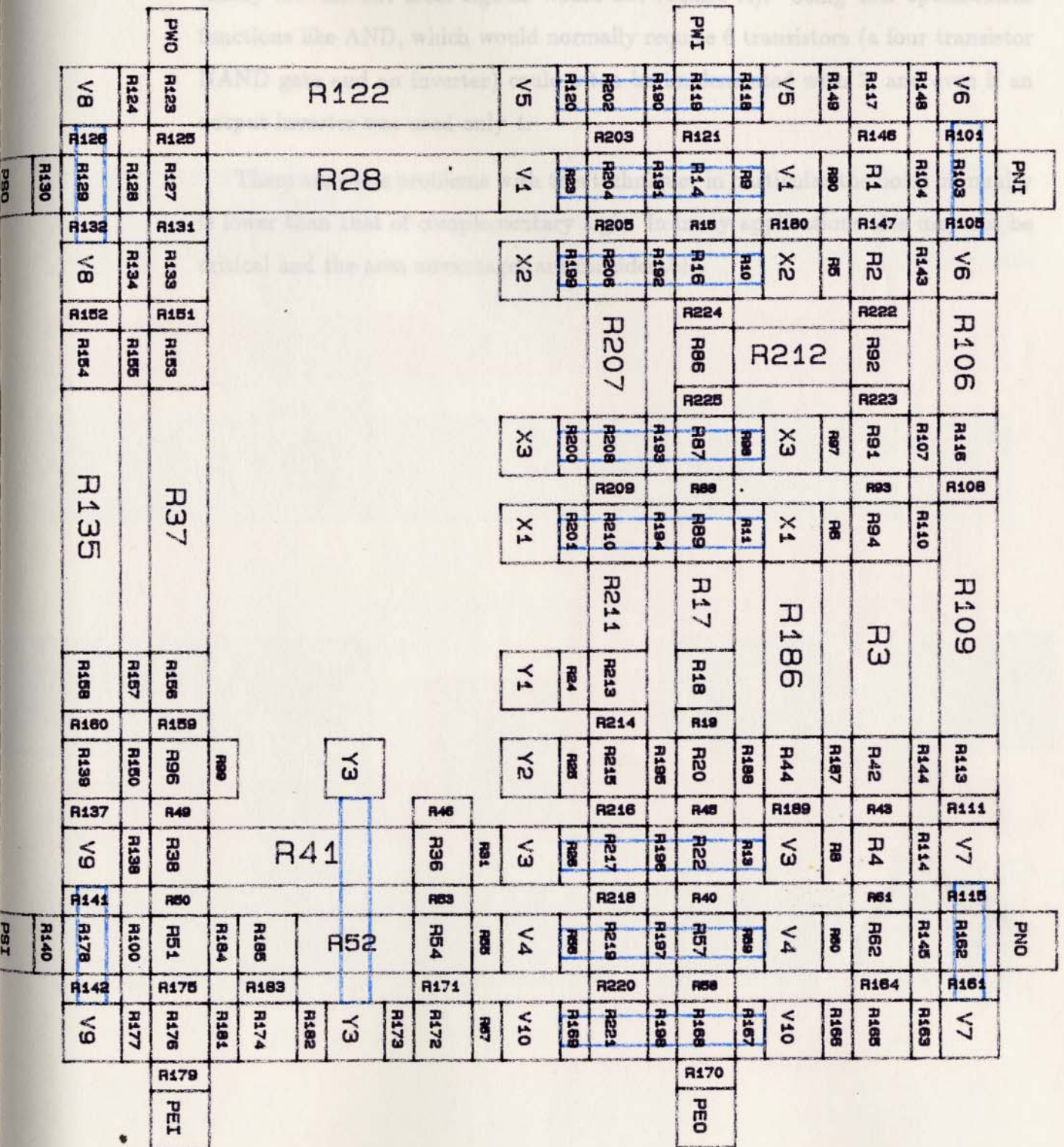


Figure 5-9: Routing Tiles.

### 5.3 Wafer Scale Version.

This section will consider methods of mapping the dynamically programmable version of the architecture into Wafer Scale Version (WSV). There are several reasons for looking at wafer scale version [Core85].

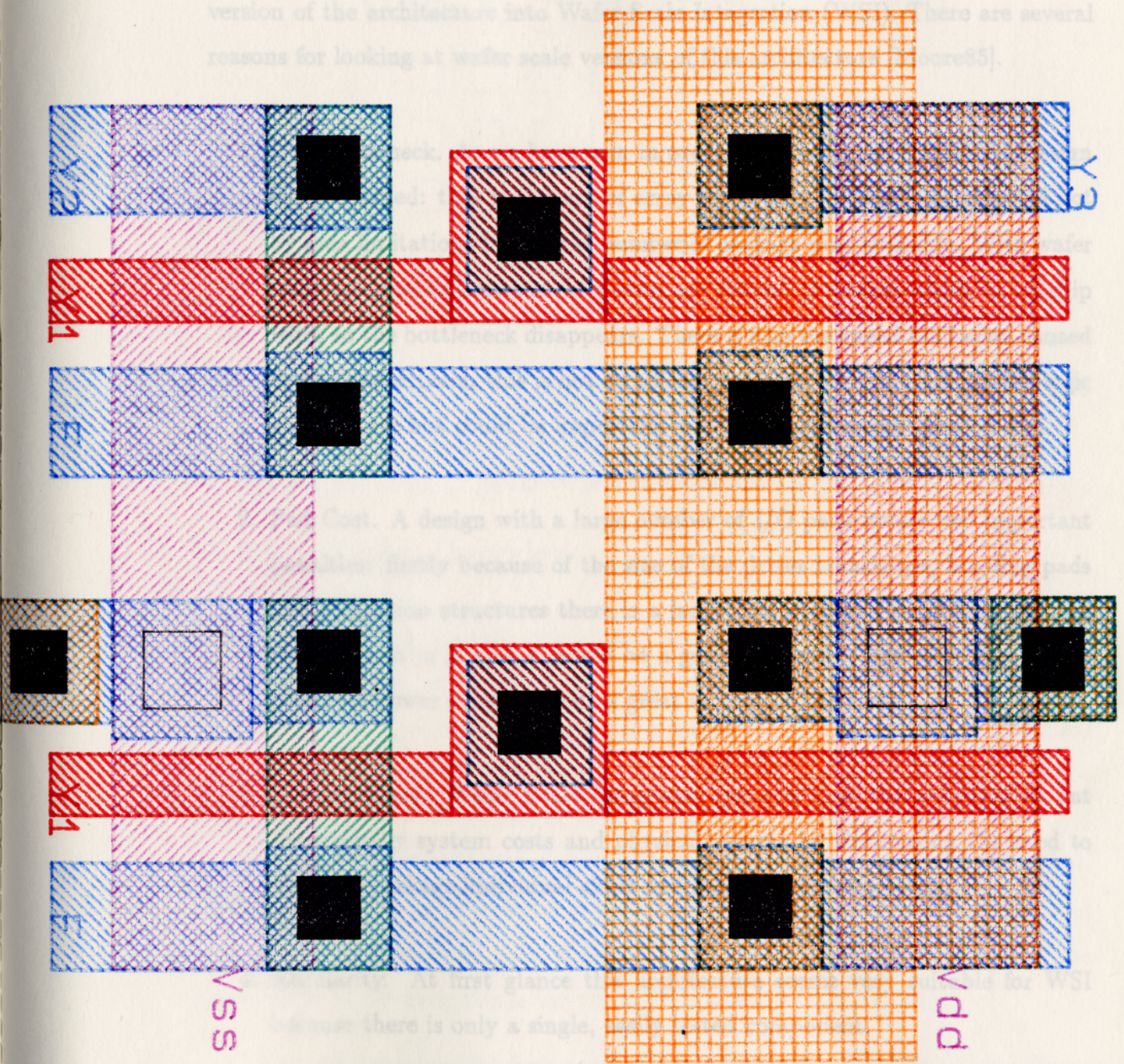


Figure 5-10: Function Block Stage Layout.